

S/N 09/785,006

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Aaron M. Schoenfeld

Examiner: Evan Pert

Serial No.: 09/785,006

Group Art Unit: 2829

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GRINDING TECHNIQUE FOR INTEGRATED CIRCUITS



Commissioner for Patents

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**RESPONSE UNDER 37 CFR § 1.111**

**REMARKS**

This responds to the Office Action mailed on October 7, 2003. Claims 11-25, 35-39 and 41-43 remain pending in this application.

**First §112 Rejections of the Claims**

Claims 18-25, 35-39, and 41-43 were rejected under 35 U.S.C. § 112, second paragraph, for indefiniteness. The Office Action states:

Applicant uses the product-by-process limitation “ground or polished,” but fails to set forth a clear scope of meaning for a *device* edge surface that *was* “ground or polished” [see MPEP 2113].

According to Merriam-Webster, the act of “grinding” is an act of “wearing down or *polishing* by friction” or “*reducing* to powder by friction.” Therefore, the act of cutting a wafer with a dicing saw is an act of *cutting* by *grinding* wafer scribe material.

(Office Action at 2.) Applicant respectfully traverses.

First, Applicant does not admit that the claimed “ground or polished” surfaces constitute product-by-process limitations. Applicant’s apparatus claims do not recite any act of “grinding” or “polishing.” Moreover, although the above language from the Office Action refers to a “surface that *was* ground,” no such language is present anywhere in the present claims. Instead, claim 18, for example, recites “surfaces . . . where the surfaces . . . are ground or polished.” Therefore, the present language therefore refers to identifiable structural attributes of the surface, rather than to earlier processes for forming such structures.

Moreover, the online edition of the same Merriam-Webster dictionary referred to in the Office Action includes—in addition to the transitive sense referred to in the above quotation from the Office Action—the following definition for the term “grind” used in an intransitive sense: “to become pulverized, polished, or sharpened by friction.” *See* Merriam-Webster Online dictionary <http://www.m-w.com/cgi-bin/dictionary> (visited on January 7, 2004). Therefore, Applicant respectfully submits that the term “ground” as recited in claim 18, for example, is fully consistent with an ordinary common dictionary definition as something that has become pulverized, polished, or sharpened by friction.

In the context of the present claims, the terms “ground or polished” refer to identifiable structural attributes. The present patent application describes a cut edge and a ground or polished edge at page 5, lines 15-18 relative to FIGS. 2 and 3. The present patent specification also describes the problems associated with cut edges versus ground edges such that one of ordinary skill in the art could recognize structural differences of a cut edge versus a ground or polished edge. (See Application at page 6, line 6 through page 7, line 5.)

The Office Action has not provided any credible evidence that one of ordinary skill in the art could not distinguish between a “cut” IC die edge and a “ground” IC die edge. In support of its position, the Office Action cites U.S. Patent Number 5,314,844 in support of its position, stating:

The ‘844 patent indicates: “The advantages of the [high speed] dicing saw method lies in the fact that the method provides a stable width of cut. Further, there are little cracks or chipping caused, and the cutting takes place at high speed, and is thus preferable in a mass production.” [emphasis added in Office Action]

Applicant says that there are *typically* “irregularities 24” (Fig. 2 + p. 6, line 6) when applicant cuts a die before “grinding or polishing” sides of the die, but well known dicing saw cutting results in “a stable width of cut” per the ‘844 patent.

(Office Action at page 3.) Applicant respectfully submits that the quoted passage from the ‘844 patent actually supports the Applicant’s position because it admits that saw cutting results in an edge that includes “little cracks or chipping”—which are substantially removed by Applicant’s grinding or polishing to provide a smooth “ground or polished” IC die edge. The Office Action further states:

The cut surface in the '844 patent is indistinguishable from applicant's claimed cut surface since applicant can admittedly only realistically "reduce" the irregularities anyways [e.g. p. 7, line 5].

Applicant describes, "treating" the sides of the die to cause a "removing" of extra scribe material and "irregularities 24." After applicant removes material and irregularities 24, the sides of the die do not have irregularities 24 shown (Fig. 3).

Yet, applicant fails to quantify the "irregularities" resulting from applicant's cut, or any quantifiable surface uniformity characteristics of die sides that are observable after subsequent grinding or polishing.

(Office Action at 3.) Applicant respectfully submits that this passage demonstrates an improper reading of the term "cut" into the rejected claims. Applicant can find no such language in these claims. Instead, claim 18, for example, recites "surfaces . . . where the surfaces . . . are ground or polished." The quoted passage further admits that the IC die edge that is not ground or polished is structurally distinguishable from an IC die edge that is ground or polished, since it states that after the material removal, "the sides of the die do not have irregularities." (*See id.*) Lastly, although the Office Action alleges that the applicant fails to quantify the irregularities before and after a "ground or polished" edge is created, it fails to present any objective evidence that one of ordinary skill in the art would not be able to distinguish a "ground or polished" surface from a surface that is not "ground or polished."

Indeed, the very '844 patent cited in the Office Action itself admits that the nature of the cracking and chipping due to saw cutting is known to one of ordinary skill in the art, as discussed above. Moreover, the present patent application refers to known processes for performing such grinding or polishing such as chemical mechanical planarization (CMP). (*See* Application at page 8, line 13.) The present patent application also describes known processes of using CMP for planarizing wafers. (*See id.* at page 4, lines 21 – 30.) Therefore, Applicant respectfully submits that one of ordinary skill in the art would have been well aware of the smoothness obtainable from known CMP, such as from process specifications for wafer planarization and/or other CMP processes. Because there is no objective evidence of record that one of ordinary skill in the art would not be able to distinguish the claimed "ground or polished" surfaces from a cut surface,

Applicant respectfully submits that these claims are sufficiently definite within the meaning of 35 U.S.C. § 112, second paragraph.

As discussed above, Applicant respectfully submits that the terms “ground or polished” are not product-by-process claim limitations. However, even if the terms “ground or polished” could somehow be interpreted as product-by-process limitations, the portion of the MPEP cited in the Office Action still supports Applicant’s position that these claim terms are not indefinite:

The structure implied by the process steps should be considered when assessing the patentability of product-by-process claims over the prior art, especially where the product can only be defined by the process steps by which the product is made, or where the manufacturing process steps would be expected to impart distinctive structural characteristics to the final product. See, e.g., *In re Garnero*, 412 F.2d 276, 279, 162 USPQ 221, 223 (CCPA 1970) (holding “interbonded by interfusion” to limit structure of the claimed composite and notice that terms such as “welded,” “intermixed,” “ground in place,” “press fitted,” and “etched” are capable of construction as structural limitations.”

*See* MPEP §2113. The “ground or polished” surfaces claimed in the present patent application connote structural differences from a cut edge, for the reasons discussed above. Therefore, even if these claims limitations were to be interpreted as product-by-process claim limitations, under the guidance of the MPEP, they are sufficiently definite to comport with the requirements of 35 U.S.C. § 112, second paragraph.

In sum, Applicant respectfully requests reconsideration and allowance of claims 18-25, 36-39 and 41-43.

#### **Second and Third §112 Rejections of the Claims**

Claim 39 and claims 17-25, 35-38, and 41-43 were separately rejected under 35 U.S.C. § 112, first paragraph, as not supported by an enabling disclosure. Additionally, the specification was objected to for not enabling polishing a bi-level edge die to get polished bilevel edges. Applicant respectfully traverses these grounds for rejection. The Office Action states:

U.S. Patent 5,196,378 explains the problem with *polishing* a die edge:

“Although edge roughness may be smoothed somewhat by polishing after dicing, the polishing process and fixturization requirements of the polishing process tend to damage the electrically active layer near the die edge” [col. 2].

Applicant fails to provide written description and explanation of how to overcome the problem of polishing a die side as taught in prior art ‘378. The generalized and generic description at the end of applicant’s disclosure does not adequately describe how to overcome the problem of polishing a die side, particularly when it has a “bi-level edge” as in the instant claims.

The act of “polishing to get a polished side of a die” tends to cause damage for a regular-sided die according to the ‘378 patent. Applicant claims a *polished bi-level* die, which has two stepped edges that need polishing, which is even more difficult than a regular die.

So how does one of ordinary skill resolve the problem of damage identified in the prior art ‘378?

Applicant says you can use CMP with tweezers and a slurry [p.8], but well known CMP does not give a “bi-level edge.” As described by applicant’s own disclosure, polishing and grinding (such as by well known CMP) is for planarizing entire wafers [p.1, lines 15-17]. Applicant doesn’t even acknowledge a problem with polishing a die edge since “the invention is not limited to a particular process of performing the grinding technique of the invention” [p. 8, lines 19-20].”

(Office Action at 4-5.)

Applicant respectfully submits that the Office Action’s reliance on the ‘378 patent as evidence of a problem with the present patent application is entirely misplaced. The ‘378 patent is entitled “METHOD OF FABRICATING AN INTEGRATED CIRCUIT HAVING ACTIVE REGIONS NEAR A DIE EDGE.” By contrast, the present application describes grinding or polishing scribe material, which does not include such active regions. (See, e.g., Application at page 1, lines 21-26 and page 5, line 27 through page 6, line 3). Therefore, the ‘378 patent’s problem of the polishing resulting in damage to active circuit areas is wholly irrelevant in the context of the present patent application.

In addition, with regard to claims 17-25, 35-38, and 41-43 the Office Action further asserts at page 6 that “the specification, while being enabling for “grinding to get a ground

edge,” does not reasonably provide enablement for “polishing a bi-level edge to get a polished bi-level edge.” However, Applicant’s specification at page 8, lines 11-22 describes:

The additional step of grinding or polishing an integrated circuit die 10 according to the invention may be performed using one of several known processes and methods. For illustration purposes, the CMP process will be briefly described. A circuit die may be held by a carrier and forced against a rotary grinding disc or polishing pad. The pad or disc is typically impregnated with a chemical or abrasive slurry which contacts the die edge to remove a portion of the scribe from the edges 18 as the pad or disc rotates. Alternatively, a mechanical gripping device such as a “tweezer” type device may be used to hold the die with an edge 18 adjacent the polishing pad or grinding disc. As will be evident to those skilled in the art, the invention is not to be limited to a particular process of performing the grinding technique of the invention, but only to the steps as described for further removing some of the remaining scribe from the edges and surfaces of an integrated circuit die.

This portion of the specification, among others, and FIGS. 1-6 enable a person of ordinary skill in the art to make and use the invention commensurate with the scope of the claims. One of ordinary skill in the art would understand that to obtain a ground or polished bi-level surface, one could use a mechanical gripping device to hold the die against a respective grinding or polishing pad, which would inherently include holding the die against an edge of such a pad to obtain a ground or polished bilevel surface.

Accordingly, Applicant respectfully requests withdrawal of these bases of rejection of these claims.

### §102 Rejection of the Claims

Claims 18-25, 35-38 and 41-43 were rejected under 35 U.S.C. § 102(e) for anticipation by Boruta (U.S. Patent No. 5,786,266). Applicant respectfully traverses. “For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference.” (emphasis added). *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566, 1567 (Fed. Cir. 1990). “The identical invention must be shown in as complete detail as is contained in the . . . claim.” *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Claims 18-21

Applicant cannot find in Boruta “at least one perimeter side surface having at least two offset planar surfaces, where the at least two offset planar surfaces are substantially parallel to each other and ground or polished” as recited or incorporated in claims 18-21.

The Office Action acknowledges that Boruta does not teach or suggest all of the claim limitations. The Office Action states at page 6 that “Figure 2D with col. 1 and 3 of Boruta *clearly anticipates* all limitations of the rejected claims *except* for calling the die edges ‘ground or polished’.”

Therefore, Boruta does not teach or suggest “at least one perimeter side surface having at least two offset planar surfaces, where the at least two offset planar surfaces are substantially parallel to each other and ground or polished” as recited in claim 18. By failing to teach such structure, Boruta does not meet the standard set forth in *In re Bond* requiring that “every element of the claimed invention must be identically shown in a single reference.” 910 F.2d at 831, 15 USPQ2d at 1566, 1567.

Moreover, Applicant respectfully submits that a polished or ground surface is not the same as a surface exposed by cutting, as recognized in Boruta at col. 4, lines 16-17. Similarly, Applicant’s own specification at page 6, lines 6-19 recognizes the problems associated with die edges formed by cutting. Accordingly, Applicant respectfully requests reconsideration and allowance of claims 18-21.

Claims 22-24

Applicant incorporates the above discussion of Boruta herein. Applicant cannot find in Boruta “at least one of the perimeter sides having at least two offset planar surfaces that are substantially parallel to each other and ground or polished to remove irregularities from each of the two offset planar surfaces” as recited or incorporated in claims 22-24. Accordingly, Applicant respectfully requests reconsideration and allowance of claims 22-24.

Claim 25

Applicant cannot find in Boruta “each perimeter side having offset perimeter planar surfaces, where the offset perimeter planar surfaces are substantially parallel to each other with

one of the offset perimeter planar surfaces extending from the first planar surface and another of the offset perimeter planar surfaces extending from the second planar surface, and each of the offset perimeter planar surfaces is a ground or polished surface" as recited or incorporated in claim 25. Accordingly, Applicant respectfully requests reconsideration and allowance of claim 25.

Claims 35-38

Applicant incorporates the above discussion of Boruta herein. Applicant cannot find in Boruta "at least one perimeter side having two or more offset planar perimeter surfaces, each of the two or more offset planar perimeter surfaces being ground or polished surfaces with one of the offset perimeter planar surfaces extending from the first planar surface and another of the offset perimeter planar surfaces extending from the second planar surface" as recited or incorporated in claims 35-38. Accordingly, Applicant respectfully requests reconsideration and allowance of claims 35-38.

Claims 41-43

Applicant incorporates the above discussion of Boruta herein. Applicant cannot find in Boruta "at least one perimeter edge having two or more offset planar surfaces, where the offset planar surfaces are substantially transverse to the first planar surface or the second planar surface with one of the offset planar surfaces extending from the first planar surface and the other of the offset planar surfaces extending from the second planar surface" as recited or incorporated in claims 41-43. Accordingly, Applicant respectfully requests reconsideration and allowance of claims 41-43.

Reservation of Right to Swear Behind References

Applicant reserves the right to swear behind any references which were cited in a rejection under 35 U.S.C. §§102(a), 102(e), 103/102(a), and 103/102(e). Statements distinguishing the claimed subject matter over the cited references are not to be interpreted as admissions that the references are prior art.

Examiner Interview

Applicant thanks Examiner Pert for his courtesy during the telephone interview with Applicant's attorney Andrew R. Peret, held on December 31, 2003, in which the Boruta reference and each of the pending rejections was discussed without reaching agreement as to the patentability of the claims.

The Examiner's Interview Summary dated December 31, 2003 states that "the claim phrase "ground or polished," with respect to distinguishable surface characteristics of semiconductor chip edges, is a relative term of degree, not defined by the specification, which renders the claims indefinite." As discussed above, Applicant respectfully submits that there is no objective evidence of record that one of ordinary skill in the art would consider a "ground or polished" surface (IC die side edge or otherwise) indefinite. Therefore, Applicant respectfully submits that this assertion amounts to a form of Official Notice. Applicant respectfully traverses any such reliance on Official Notice and respectfully requests that the Examiner either (1) cite references in support of this position pursuant to M.P.E.P. § 2144.03, or (2) submit an affidavit as required by 37 C.F.R. § 1.104(d)(2) to support the position.

As discussed above, a polished or ground surface is not the same as a surface exposed by cutting. The specification in Boruta recognizes this at col. 4, lines 16-17. The portion of the '844 patent quoted by the Examiner recognizes this. Applicant's own specification at page 6, lines 6-19, also recognizes this.

The Interview Summary further states that:

During the interview, applicant indicated that the instant claimed product is formed differently because it is separated from a wafer by cutting, FOLLOWED by a treatment to achieve "ground or polished," which is a different methodology than just a grinding type of cut. The examiner agrees that the methodology is different, but the instant claims are not method claims: The instant claims are product claims and the scope of the claimed final product does not depend on how a ground edge was achieved, but rather the fact that there is a ground edge [MPEP 2113].

Applicant respectfully traverses these assertions for two reasons. First, Applicant asserts that the claimed polished or ground surface is structurally different from a surface exposed by cutting. Applicant does NOT assert or admit that the claims cover only a

surface formed by cutting and then treating. Second, MPEP 2113 recognizes terms such as ground or polished as proper structural terms, as discussed above.

### CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's below-signing attorney facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 9 day of January, 2004.

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